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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,541	06/23/2003	Takeshi Sakata		5764

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,541	SAKATA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *8-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/349,761.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-7) in the reply filed on 07/16/2004 is acknowledged.

Claims 8-23 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected inventions, there being no allowable generic or linking claim.

Election was made **without** traverse in the reply filed on 07/16/2004.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami, Shuji et al. (US 5471427 A, hereafter referred to Murakami) in view of Harper; Samuel D. (US 3633175 A).

35 U.S.C. 103(a) rejection of claim 1.

Murakami teaches a fuse sets for a nxn memory array with n^2 memory cells. The fuse arrangement provides n fuses (See Figure 1, Murakami). The Examiner would like to point out that a fuse is capable of storing only one bit of information. The fuse circuits in Figure 1 (in Murakami) are capable of storing NS>=2 defective addresses.

However Murakami does not explicitly teach that the defective address storing circuit includes $ND = 2^{NA}$ storage elements.

The examiner would like to point out that if $n = 2^{NA}$ for some number NA, then n = ND in which case the defective address storing circuit includes $n = ND = 2^{NA}$ storage elements, therefore Figure 1 of Murakami is a generalization of the Applicant's claim 1, hence restricting $n = ND = 2^{NA}$ does not deviate from the scope or the intent of the teachings of Murakami.

However Murakami does not explicitly teach the specific use of $ND = 2^{NA}$ storage elements.

Harper, in an analogous art, teaches use of $ND = 2^{NA}$ storage elements (col. 2, lines 63-70, Harper).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Murakami with the teachings of Harper by including use

of ND = 2^{NA} storage elements. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of ND = 2^{NA} storage elements would have provided a means for optimizing a binary address space for memory, that is; there are exactly as many address as storage elements, which reduces the storage requirements for address to exactly the number of addresses necessary to address the memory.

35 U.S.C. 103(a) rejection of claim 2.

Murakami teaches the use of fuses (i.e., programmable devices) in Figure 1, Murakami.

35 U.S.C. 103(a) rejection of claim 3.

The fuses in Figure 1 of Murakami are used to represent two states and are sequentially ordered according to column addresses.

35 U.S.C. 103(a) rejection of claim 4.

Selecting NA or NS to satisfy the equation in the Applicant's claim 4, does not deviate from the scope or intent of Murakami's teachings since NS and NA would still fall within an acceptable range of value for NS and NA in the Murakami patent.

35 U.S.C. 103(a) rejection of claim 5.

See Figure 1 of Murakami.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami, Shuji (US 5471427 A) and Harper; Samuel D. (US 3633175 A) in view of Kato, Hideo (US 6249850 B1).

Murakami and Harper substantially teaches the claimed invention described in claims 1-5 (as rejected above).

However Murakami and Harper does not explicitly teach that address storage is included in the redundancy circuitry.

Kato, in an analogous art, teaches that address storage is included in the redundancy circuitry (see Figure 1, Kato).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Murakami and Harper with the teachings of Kato including address storage with the redundancy circuitry. This modification would have been obvious to one of ordinary skill in the art, at the time of the invention, because one of ordinary skill in the art at the time of the invention would have recognized that including address storage with the redundancy circuitry would provide the opportunity to improve fault tolerance in system applications requiring error-free data.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami, Shuji (US 5471427 A) and Harper; Samuel D. (US 3633175 A) in view of Cloud, Eugene H. et al. (US 6119251 A, hereafter referred to as Cloud).

Murakami and Harper substantially teach the claimed invention described in claims 1-5 (as rejected above).

However Murakami and Harper do not explicitly teach address storage using a fuse circuit.

Cloud, in an analogous art, teaches:

> "The external testing unit may, for example, store the failed addresses in a database searchable by a unique DRAM ID code. The failed addresses may be repaired by known DRAM repair techniques, such as replacing failed addresses with redundant rows/columns using laser or electrical fuses" (col. 7, lines46-51, Cloud).

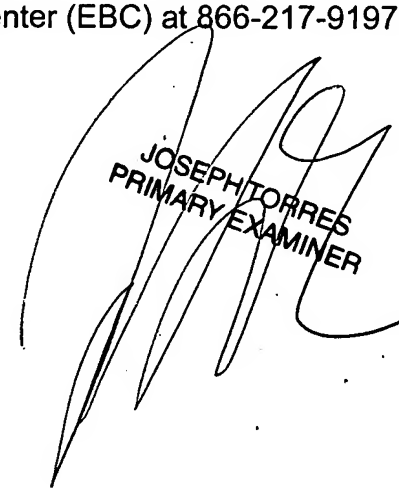
Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Murakami and Harper with the teachings of Cloud including fuse circuits for address storage. This modification would have been obvious to one of ordinary skill in the art, at the time of the invention, because one of ordinary skill in the art at the time of the invention would have recognized that fuse circuits would provide the opportunity to improve fault tolerance in system applications requiring error-free data.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133